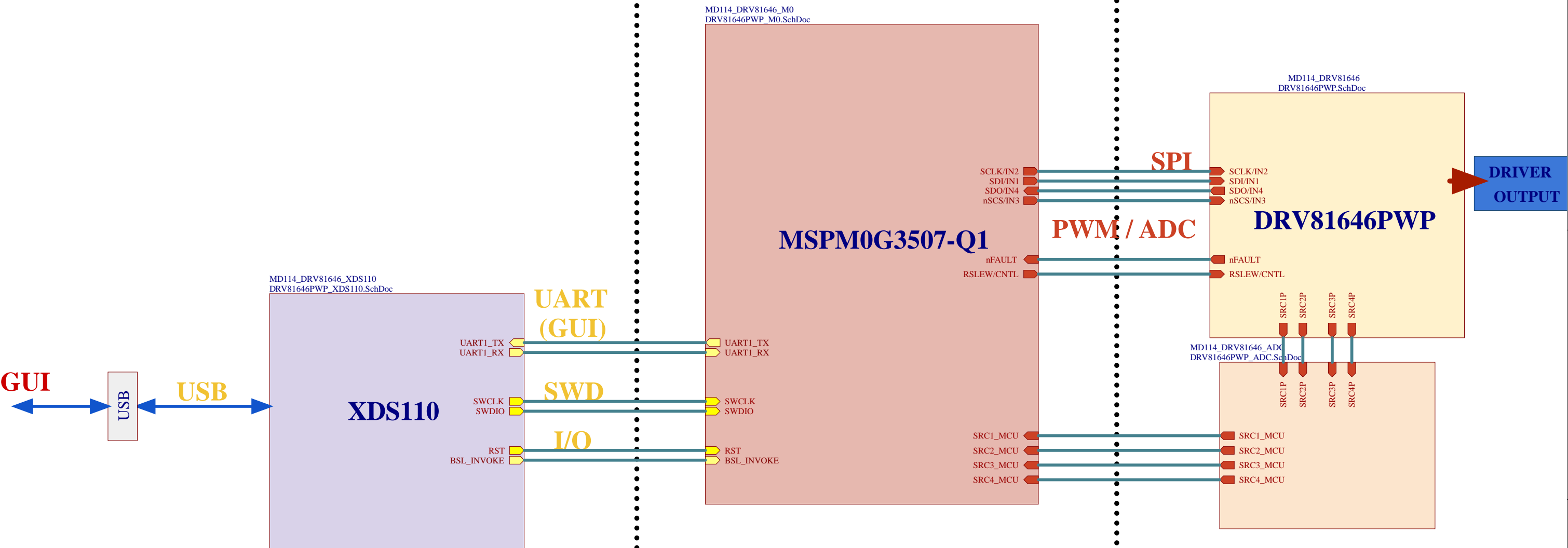


DRV81646PWP TOP LEVEL SCHEMATIC

INTERFACE/DEBUGGING

PROCESSING

DRIVER + OUTPUTS

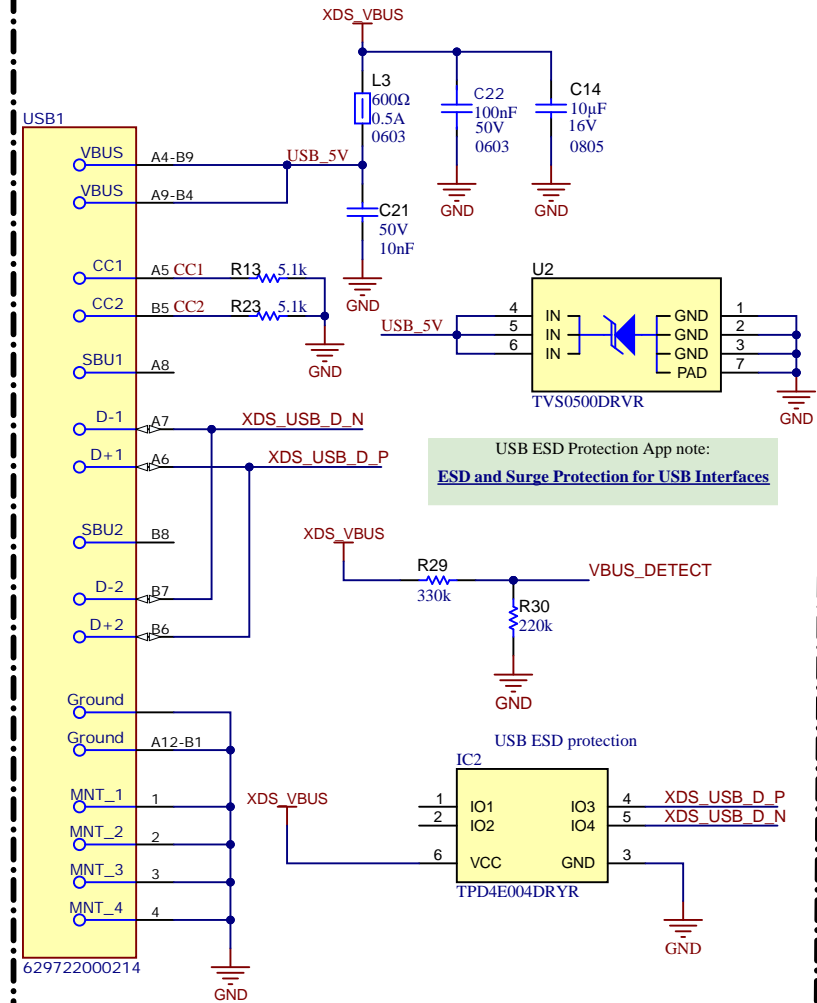


MD114_DRV81646_Hardware
DRV81646PWP_Hardware.SchDoc

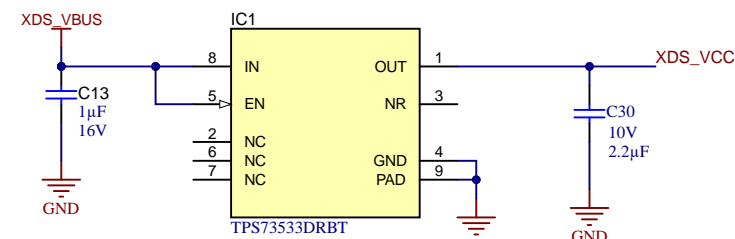
Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

Orderable: DRV81646EVM	Designed for: Public Release	Mod. Date: 5/19/2025
TID #: N/A	Project Title: DRV81646PWP	
Number: MD114-001	Rev: E1	Sheet Title: TOP LEVEL SCHEMATIC
SVN Rev: Not in version control	Assembly Variant: DRV81646PWP	Sheet: 0 of 5
Drawn By: Mojtaba Afshar	File: DRV81646PWP_Top_Level.SchDoc	Size: B
Engineer: Mojtaba Afshar	Contact: http://www.ti.com/support	

USB-C Interface, ESD Protection



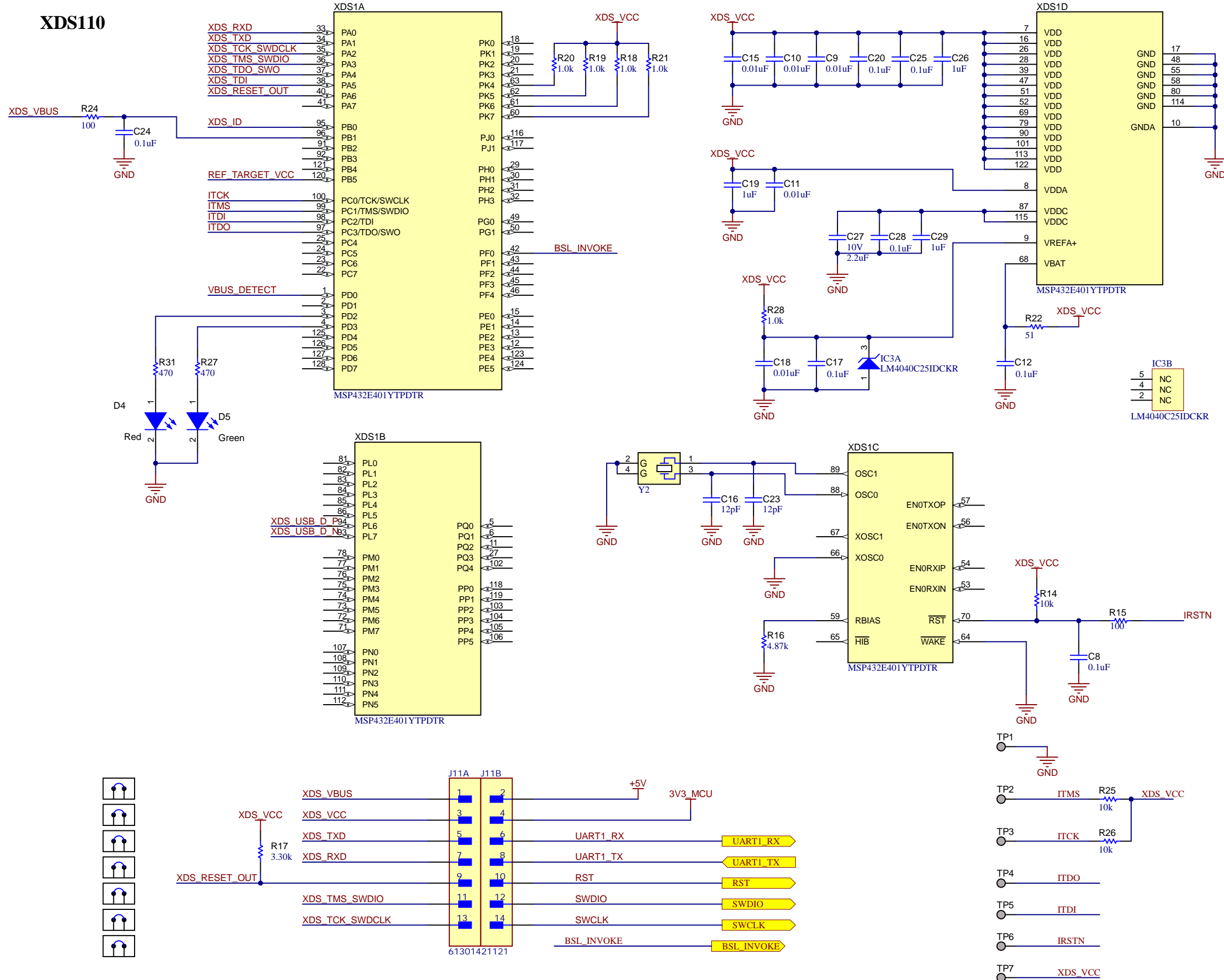
3.3V LDO



500-mA
Low IQ: 45 µA
Stable With a Ceramic, 2.2-µF, Low-ESR Output Capacitor

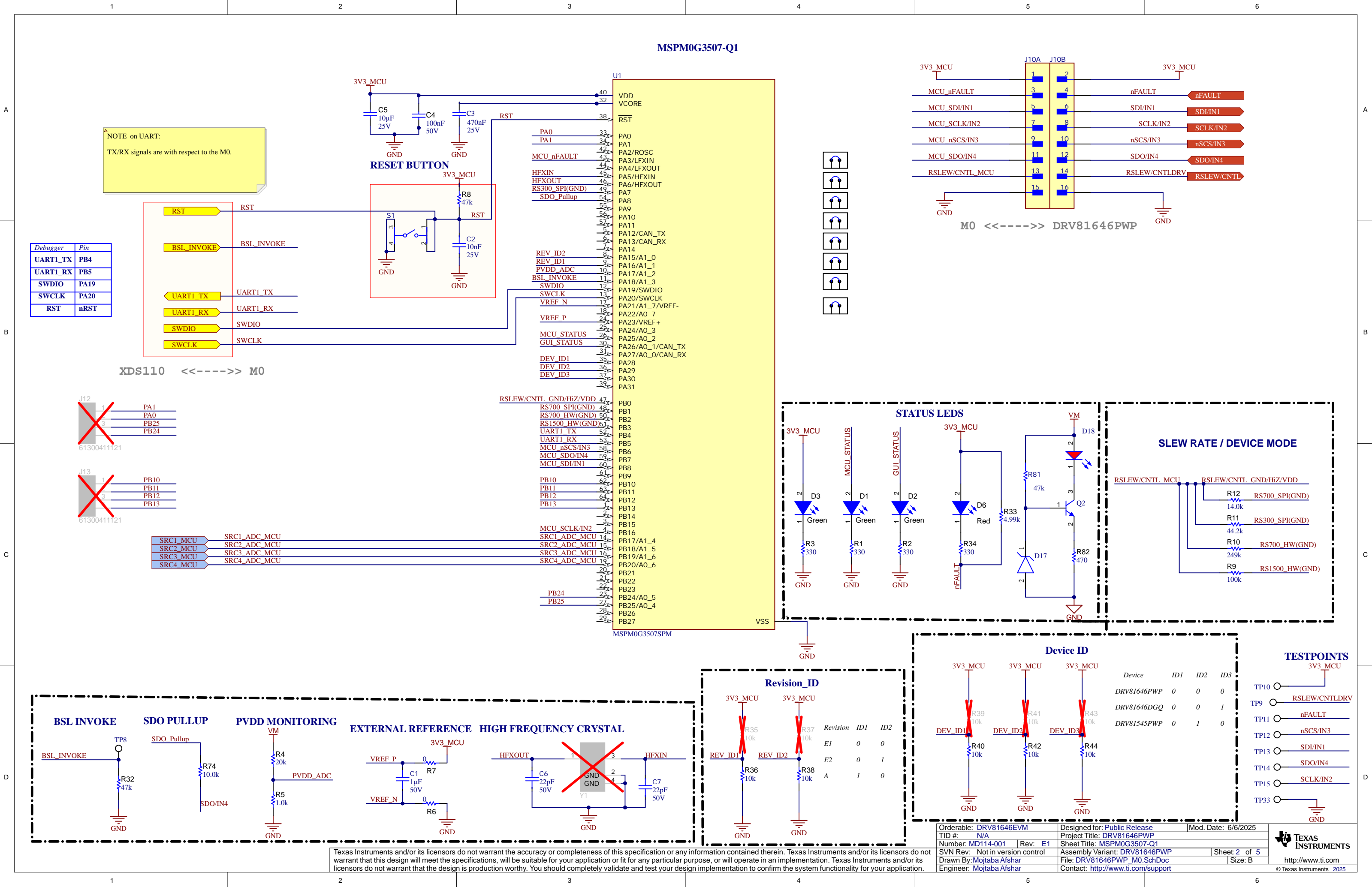
XDS--
LDO current IINRUSH Inrush current 50 max 250 mA
Peripheral Current Consumption

XDS110



XDS110 <-----> LaunchPad

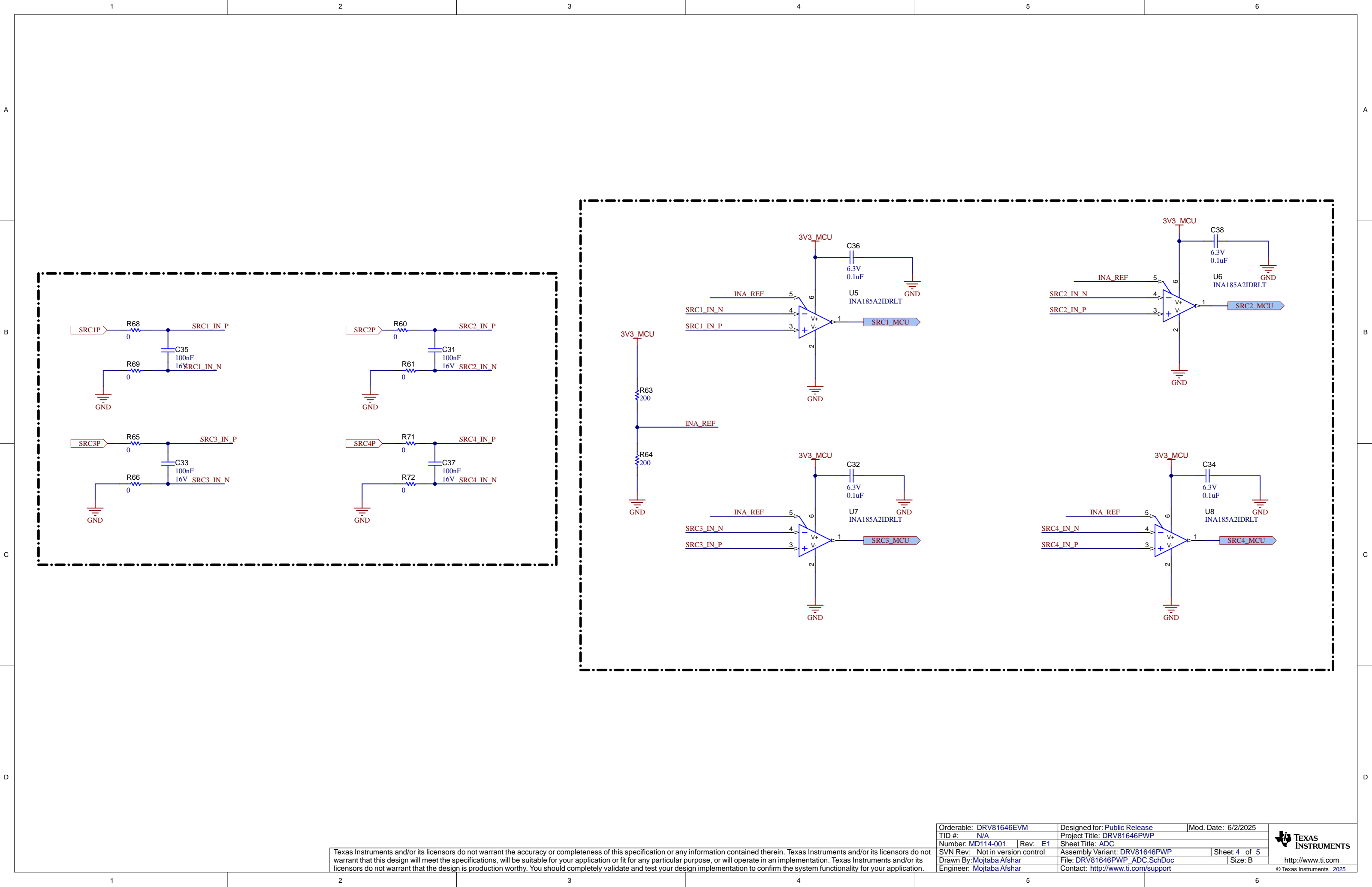
Orderable: DRV81646EVM	Designed for: Public Release	Mod. Date: 5/18/2025
TID #: N/A	Project Title: DRV81646PWP	
Number: MD114-001	Rev: E1	Sheet Title: XDS110
SVN Rev: Not in version control	Assembly Variant: DRV81646PWP	Sheet: 1 of 5
Drawn By: Mojtaba Afshar	File: DRV81646PWP_XDS110.SchDoc	Size: B
Engineer: Mojtaba Afshar	Contact: http://www.ti.com/support	





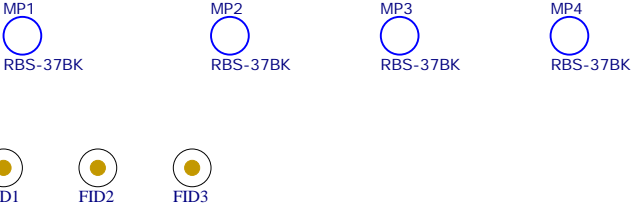
RILIM Resistor between ILIM and SGND
 $0 < \text{RILIM} < 20\text{k}\Omega$: ILIM Limited to 3A
 $30\text{k}\Omega \leq \text{RILIM} < 120\text{k}\Omega$: ILIM Limited to 60 / RILIM (k Ω)
 $120\text{k}\Omega \leq \text{RILIM}$: ILIM Limited to 60 / RILIM (k Ω). Linearity is not guaranteed.

COD/INRUSH
 $0 \leq \text{RCOD} < 20\text{k}\Omega$: Disabled
 $60\text{k}\Omega \leq \text{RCOD} \leq 240\text{k}\Omega \rightarrow \text{tCOD (ms)} = \text{RCOD(k}\Omega)/120$
 Unconnected: INRUSH mode




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Orderable: DRV81646EVM	Designed for: Public Release	Mod. Date: 6/2/2025
TID #: N/A	Project Title: DRV81646PWP	
Number: MD114-001	Rev: E1	Sheet Title: ADC
SVN Rev: Not in version control	Assembly Variant: DRV81646PWP	Sheet: 4 of 5
Drawn By: Mojtaba Afshar	File: DRV81646PWP_ADC.SchDoc	Size: B
Engineer: Mojtaba Afshar	Contact: http://www.ti.com/support	




PCB Number: MD114-001
PCB Rev: E1

PCB
LOGO
Texas Instruments


CE Mark

PCB
LOGO
FCC disclaimer

PCB
LOGO
WEEE logo


CAUTION HOT SURFACE

PCB
LOGO
CAUTION. READ USER GUIDE BEFORE USE

Variant/Label Table	
Variant	Label Text
001	DRV8000-Q1EVM

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.